ABSTRACT

A hybrid tester architecture for testing a plurality of semiconductor devices in parallel is disclosed. The hybrid tester architecture includes per-pin formatting circuitry having data input circuitry and clock input circuitry and shared timing circuitry coupled to the clock input circuitry. The shared timing circuitry generates programmed timing signals. Per-pin data circuitry couples to the data input circuitry and generates drive data and expected data values associated with each individual device pin. The per-pin formatting circuitry responds to the programmed timing signals to produce tester waveforms in accordance with the per-pin data.